

**In System Programming solution for Intel
Architecture Reference and Validation
boards using SPI firmware storage**

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In System Programming - Introduction

To offer highest flexibility for BIOS update during development, debugging, production and repairing, Intel has co-worked with DediProg to define and develop an innovative In System Programming solution of updating BIOS on board. This solution is,

- a. Easy to use - no need to unsolder the memory part
- b. Cheap - no need of socket
- c. Ensure the best SPI signals quality - memory soldered on board

ISP Features: Update your main BIOS memories soldered on motherboard by using dedicated ISP programmer: **SF100** or **SF100+**. When connected to the motherboard, the **SF100** programmer can control the Serial Flash to read or update its content.

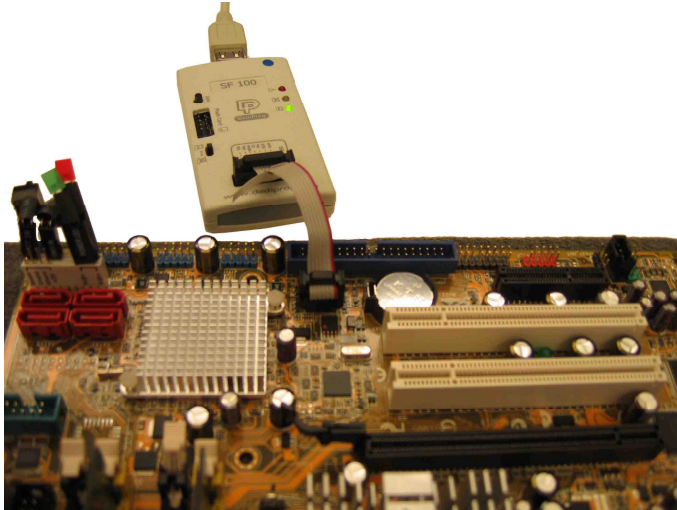
Requirements:

- Motherboard must be designed with MOSFET protection on the SPI bus to isolate the ICH Southbridge during the serial Flash update and to avoid conflict with the programmer.

Benefits:

- Easy BIOS update
- Very fast update (10sec to 30 sec)
- Flexible memory content access and update to improve BIOS development, debugging time and reduce time to market

Fig 1: In System Programming update

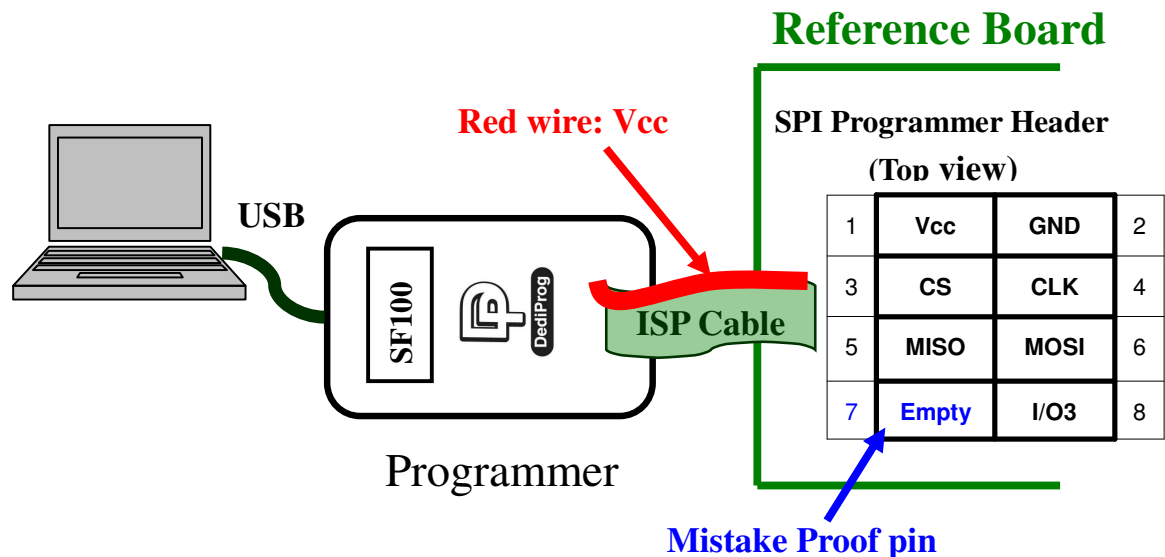


ISP method for IA Reference and Validation boards

2.1. SF100 programmer connection

The programmer can be easily connected on the board ISP connector as illustrated on the Figure 2 below:

Fig 2: ISP Connector pin out



Tab 1: Description of the signals:

Pin	Name of signal	Description
1, 2	Vcc, Gnd	Vcc and Gnd supplied from the programmer to the Serial Flash
3, 4, 5, 6	CS, CLK, MISO, MOSI	SPI signals
8	IO3	Could be used to reset the Chipset or switch off the MOSFET
7	Mistake proof pin	Prevention from wrong connection

Note: Pins 7 and 8 can be removed from the connector footprint saving area on the board. In this case ensure the cable and connector orientation are matching when connecting.

2.2. Configure Board for BIOS update

The board should be designed to avoid any conflicts between the programmer and the ICH Southbridge SPI Interface during the update.

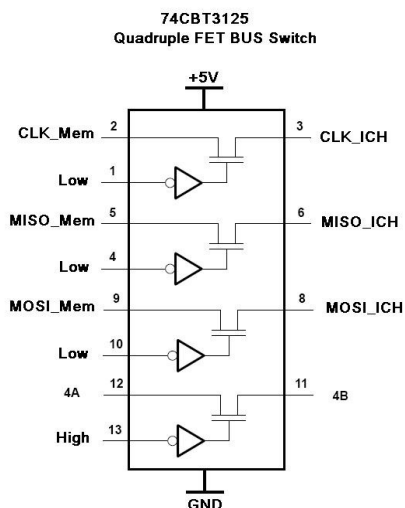
1) Clock, MISO and MOSI isolation:

We can use a simple quadruple FET Bus Switch (eg:74CBT3125 or 74CBT3306) in order to isolate the ICH SPI Interface during the BIOS update from the programmer. When the motherboard rails are not ON, FET Bus switch will open the individual MOSFETs so that the programmer and the memories will be isolated from the ICH.

It has been checked out on Intel customer reference platforms that the MOSFET switch does not introduce unnecessary voltage drop or signal integrity concerns when the motherboard is operating. However it is highly recommended that the system designer should select the MOSFET switch with the lowest RdsON. Designer should also simulate and ensure the SI compliance for the specific topology of implementation compared against the Intel platform design guide.

Additional MOSFET switches or unused transistors in the MOSFET switch can be utilized to provide isolation for the Power supply voltage and Chip selects for increased flexibility in system design. In this case, the system designer should verify the MOSFET can sustain the required amount of current through it.

Fig 3: quadruple FET Bus Switch



Normal mode:

- Motherboard rails are ON and SPI signals from Memory devices are connected to

ICH Southbridge for the normal operation through the MOSFETs

ISP update mode:

- Motherboard rails are not ON and SPI signals from memory are disconnected from ICH Southbridge (MOSFETs OPEN).

2) Motherboard 3.3V and Chip Select isolation:

Intel is using the same MOSFET to isolate the main board 3.3V power supply from the SPI memory power supply provided by the SF100 programmer. When the power rails on the mother board are OFF, MOSFET switch provides isolation for this power supply.

Further, Individual chip selects from the ICH are also isolated using the MOSFET switch while programming the SPI memory devices.

Normal mode:

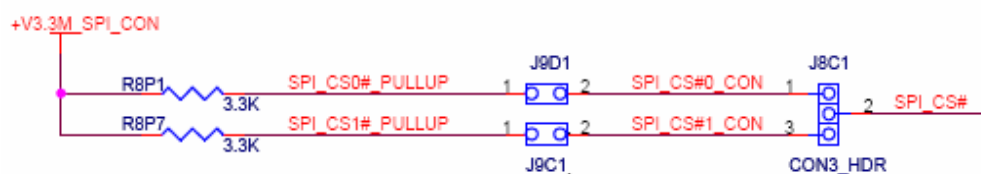
- When MOSFET is ON 3.3V on mother board will get connected to the SPI memory power supply. The voltage drop has been measured to be within specs when passing through the FETs on Intel platforms.

Note: A DIODE also can be used to auto isolate the 3.3V from the main board 3.3V power when the SF100 plugging in.

3) Memory selection for updating BIOS:

Intel motherboard has been designed to work on two different serial Flash soldered on board. User can select which memory has to be updated by the programmer by using a jumper strapping mechanism like in the following example,

Fig 4: Jumper selection of SPI device



Normal mode:

- J9D1 and J9C1 open since ICH Southbridge signals are push-pull type and does not need external pull ups for the memory device Chip selects
- J8C1 (1-2) and (2-3) open

ISP update mode:

- J9D1 and J9C1 are closed to ensure SPI memory device Chip select is disabled by default and will help prevent corruption of the device by spurious inputs.
- J8C1 (1-2 closed) to update the Device0
- J8C1 (2-3 closed) to update the Device1

2.3. Update Firmware

The following section will detail how to perform In System Programming for one of the memories soldered on the board with a Step by Step approach:

- 1) Switch OFF the ATX power supply and disconnect the ATX power supply from the board.
- 2) Close the strap J9D1 and J9C1 to provide pull up on chip select.
- 3) Select the memory to be updated with the J8C1 strap: (1-2)=Device0 or (2-3)=Device1
- 4) Connect the SF100 programmer to the connector
- 5) Connect the SF100 programmer USB cable to the Host computer
- 6) Open the DediProg Software in the computer (automatic detection of the serial Flash)
- 7) Select the Bios file to be programmed by clicking the “file” Icon and browser
- 8) Start the bios Update by clicking the “batch” Icon if configured with Erase, programming and verify operations.

Fig 5: software update interface: 8) and 9)



Now, Configure the board for Normal operation as below:

- 1) Open the straps J9D1 and J9C1
- 2) Open the strap J8C1
- 3) Switch On the ATX/AC Brick power supply to boot the board

3. Contacts

For more information on the Serial flash programmers, on the In System Programming methods or Backup boot flash methods please contact:

DediProg:

Technical support: support@dediprog.com

Sale information: sales@dediprog.com or fax to +886-2-6618-1320

Web site: www.DediProg.com

Contact DediProg support if you want to investigate all the Bios update solutions applicable to your own motherboard to benefit of the bios update flexibility for development, production and repairing.